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14. (New) The semiconductor die as recited in claim 11, wherein the perimeter edge has a ground surface.

15. (New) A semiconductor die comprising:

a first planar surface having circuitry thereon;

a second planar surface opposite the first planar surface;

one or more perimeter edges disposed between the first planar surface and the second planar surface; and

at least one perimeter edge having a treated surface, the entire at least one perimeter edge having a substantially smooth surface; and

the first planar surface and the second planar surface of the semiconductor die have an overall rectangular shape.

16. (New) The semiconductor die as recited in claim 15, wherein the entire edge comprises a ground surface.

17. (New) The semiconductor die as recited in claim 15, wherein the entire edge comprises a polished surface.

18. (New) A semiconductor die comprising:

a first planar surface having circuitry thereon;

a second planar surface opposite the first planar surface;

one or more perimeter edges disposed between the first planar surface and the second planar surface; and

at least one perimeter edge having offset planar edges, where the planar edges are substantially parallel to each other.

19. (New) The semiconductor die as recited in claim 18, wherein the semiconductor die comprises a rectangular die.

20. (New) The semiconductor die as recited in claim 18, wherein each perimeter edge has offset planar edges.

21. (New) The semiconductor die as recited in claim 18, wherein each planar edge is substantially smooth and flat.

22. (New) A semiconductor die comprising:

a first planar surface having circuitry thereon;

a second planar surface opposite the first planar surface;

one or more perimeter edges disposed between the first planar surface and the second planar surface; and

means for providing the perimeter edge of the semiconductor die with one or more substantially flat surfaces.

23. (New) The semiconductor die as recited in claim 22, wherein the entire perimeter edge is a substantially smooth surface.

24. (New) The semiconductor die as recited in claim 22, wherein the at least one perimeter edge has offset planar edges, where the planar edges are each substantially smooth and are substantially parallel to each other.

25. (New) A semiconductor die comprising:

a first planar surface having circuitry thereon;

a second planar surface opposite the first planar surface;

one or more perimeter edges disposed between the first planar surface and the second planar surface;

each perimeter edge having offset planar edges, where the planar edges are substantially parallel to each other, and the planar edges are treated, substantially smooth surfaces; and

the semiconductor die has an overall rectangular footprint.

26. (New) A method of producing a semiconductor die comprising:

cutting a wafer of material, the wafer having a first planar surface and a second planar surface opposite the first planar surface;

forming circuitry on the first planar surface;

dividing the wafer into a plurality of semiconductor dies, each semiconductor die having one or more side edges; and

removing at least a portion of the side edges and forming an entirely flat side edge.

27. (New) The method as recited in claim 26, wherein dividing the wafer into a plurality of semiconductor dies comprises dividing the wafer into a plurality of rectangular dies.

28. (New) The method as recited in claim 26, further comprising decreasing a width and length of the semiconductor die.

29. (New) The method as recited in claim 26, further comprising polishing each side edge of the semiconductor die.

30. (New) A method of producing a semiconductor die comprising:

cutting a wafer of material, the wafer having a first planar surface and a second planar surface opposite the first planar surface;

forming circuitry on the first planar surface;

dividing the wafer into a plurality of semiconductor dies, each semiconductor die having one or more side edges; and

treating one or more of the side edges and forming one or more side edges having offset planar edges.

31. (New) The method as recited in claim 30, wherein treating one or more of the side edges comprises polishing one or more of the side edges.

32. (New) The method as recited in claim 30, wherein dividing the wafer into a plurality of semiconductor dies comprises dividing the wafer into a plurality of rectangular dies.

33. (New) The method as recited in claim 30, wherein treating one or more of the side edges includes removing material from an entire surface of one or more side edges, and removing material from a portion of the entire surface.

34. (New) The method as recited in claim 30, wherein forming the one or more side edges includes forming each planar edge with a substantially flat, smooth surface.

Claims 11-34 are now pending in this application. The Examiner is invited to contact the below-signed attorney with any questions concerning the present applicaiton.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 14 day of May, 2001.

Tina Pugh
Name

_____
Signature